Capacitors used in coupling and DC blocking applications serve to couple RF energy from one part of a circuit to another and are implemented as series elements. Proper selection of coupling capacitors insures the maximum transfer of RF energy. All capacitors will block dc by definition; however, considerations for satisfying the requirements of a coupling application depend on various frequency-dependent parameters that must be taken into account beforehand.

Figure 1 illustrates two RF amplifier stages operating in a 50-ohm network interconnected by coupling capacitor C0. Table 1 outlines several device options for achieving interstage coupling at various wireless frequencies. Electrical parameters such as series resonance, impedance, insertion loss, and equivalent series resistance must be evaluated in order to achieve an optimal coupling solution.

**Table 1: Examples of coupling capacitors & associated parameters**

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Device Options</th>
<th>FSR (MHz)</th>
<th>Insertion Loss S21 (dB)</th>
<th>ESR (ohms)</th>
<th>Package Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>900</td>
<td>100A101 - 100 pF</td>
<td>1000</td>
<td>&lt;0.1</td>
<td>0.072</td>
<td>55 mil x 55 mil</td>
</tr>
<tr>
<td>1900</td>
<td>100A270 - 27 pF</td>
<td>1870</td>
<td>&lt;0.1</td>
<td>0.161</td>
<td>55 mil x 55 mil</td>
</tr>
<tr>
<td>2400</td>
<td>100A160 - 16 pF</td>
<td>2410</td>
<td>&lt;0.1</td>
<td>0.218</td>
<td>55 mil x 55 mil</td>
</tr>
</tbody>
</table>

**Figure 1: Interstage coupling block diagram**

Note: Coupling capacitor C0 in Figure 1 is represented with its equivalent series resistance (ESR) denoted as R_S, equivalent series inductance (ESL) denoted as L_S, and parallel capacitance C_P, associated with the parallel resonant frequency (F_P). Capacitors used in coupling and dc blocking applications serve to couple RF energy from one part of a circuit to another and are implemented as series elements. Proper selection of coupling capacitors insures the maximum transfer of RF energy. All capacitors will block dc by definition; however, considerations for satisfying the requirements of a coupling application depend on various frequency-dependent parameters that must be taken into account beforehand.

**Figure 2: Impedance vs. Frequency for ATC100A101 (100 pF)**

As seen in Figure 2 the net impedance below F_SR is capacitive and is dominated by 1/ohmC yielding a hyperbolic curve for frequencies less than F_SR. Conversely, the net impedance above F_SR is inductive and is dominated by inductor yielding a linear line segment for frequencies greater than F_SR.

**Table 1: Examples of coupling capacitors & associated parameters**

A capacitor’s series resonant frequency (F_SR) also referred to as self-resonance, occurs at

F_SR = \frac{1}{2\pi \sqrt{L_C}}.

At this frequency the capacitor’s net reactance is zero and the impedance is equal to the ESR. As shown in Table 1, an ATC100A101, (100 pF) porcelain capacitor has an F_SR of 1000 MHz with a corresponding ESR of 0.072 ohms. At this frequency the capacitor will provide its lowest impedance path required for optimal coupling. In contrast the impedance of a capacitor at its parallel resonant frequency (F_P) can be precipitously high. By assessing the magnitude of S21 vs. frequency for a given capacitor, excessive losses associated with F_SR at the operating frequency can be readily observed. In coupling applications a capacitor’s F_SR can usually be exceeded without posing a problem as long as the net impedance remains low.

**Net Impedance**

The magnitude of a capacitor’s impedance is equal to

\sqrt{ESR^2 + (XL - XC)^2}.

As seen by this relationship a capacitor’s impedance is significantly influenced by its net reactance (XC - XL). It is important to know the magnitude of the impedance throughout the desired passband. A properly selected coupling capacitor will exhibit suitably low impedance at these frequencies.

**Figure 3: Insertion loss vs. Frequency for ATC100A101, 100 pF chip capacitor in flat mount orientation**

Figure 3 illustrates the insertion loss characteristic of an ATC100A101 (100pF) capacitor. The sample was measured in a series through configuration from 50 MHz to 4 GHz with the capacitor’s electrodes parallel to the substrate, i.e. flat mount orientation. As seen in figure 3 the capacitor’s insertion loss is less than 0.1 dB between 200 MHz to 1.5 GHz. By edge mounting the capacitor, i.e. electrodes perpendicular to the substrate, the first parallel resonant notch at 1.6 GHz will be suppressed. As a result the usable frequency range will be extended to approximately 2.4 GHz. In this orientation the same capacitor can be used to include all of the wireless frequencies in a broadband coupling application.

**ESR and Q**

A capacitor’s quality factor (Q) is numerically equal to the ratio of its net reactance (XC - XL) to its equivalent series resistance

Q = \frac{|XC - XL|}{ESR}.

From this expression it can be seen that the capacitor’s Q varies inversely to its ESR and directly with the net reactance. A capacitor’s ESR should be known at all frequencies within the passband, especially at frequencies above the capacitor’s series resonant frequency. At the frequency where the electrode thickness is at least one skin depth the ESR will increase as the \sqrt{C}. Accordingly, the ESR will increase in this fashion for increasing frequencies and may become the dominant loss factor. As previously mentioned an attenuation notch will occur at the capacitor’s F_SR, the depth of which is inversely proportional to the ESR. Therefore the capacitor’s ESR will largely determine the depth of the attenuation notch at the parallel resonant frequency.

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